NATIONAL UNIVERSITY OF SCIENCES AND TECHNOLOGY
COLLEGE OF ELECTRICAL AND MECHANICAL ENGINEERING

DIGITAL SYSTEM DESIGN
LAB HW 1
DE31 (EE)

Submission: 19th Sep 2011

Combinational System Design

Objective: The objective of the Lab is to make students understand the link between their previously learned knowledge with design and implementation of a digital system in Verilog. This Lab also helps students gain some confidence with basic Verilog syntax.

Design Problem:

1. There are three input signals and two output signals as shown in Figure 1.
2. Input signals change on the rising edge of the clock signal 'clk'.
3. Design digital logic that generates the outputs for the corresponding inputs as shown in the figure.
4. **Show ALL the rough work that leads up to the design.**

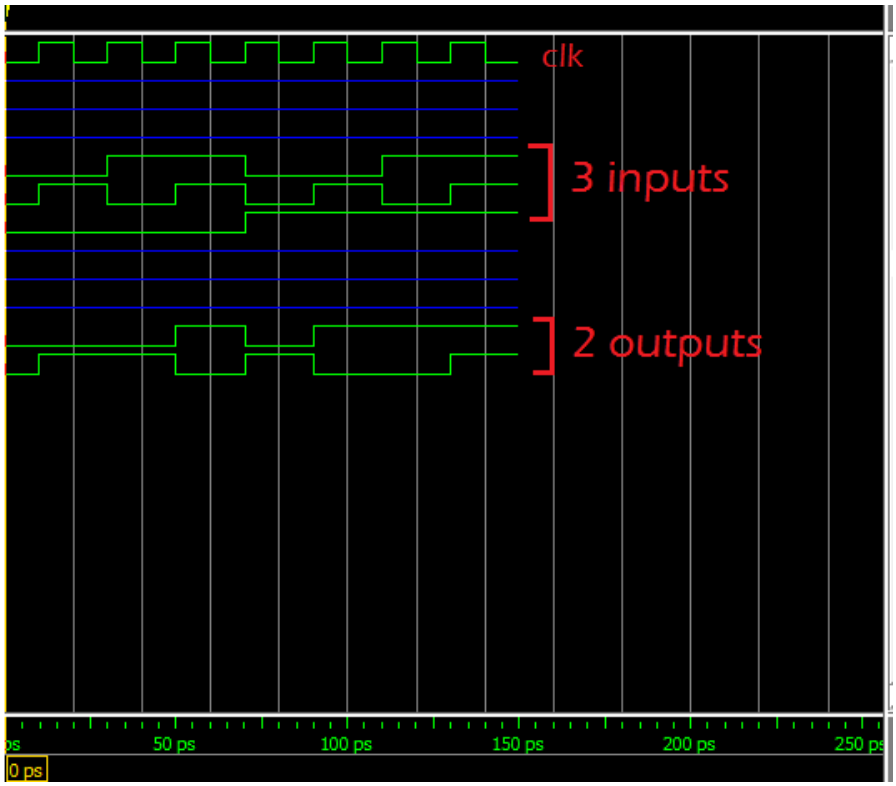

Figure 1: Waveforms for the design problem